AMENDMENTS TO THE CLAIMS

Please cancel claims 5 and 6 without prejudice or disclaimer of the underlying subject matter and amend claims 3 and 4 as set forth below:

3. (CURRENTLY AMENDED) A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

a first inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said first inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said first inter-layer insulation film;

a plug having conductivity and filling internal portions of said first connection hole and said second connection hole;

a second inter-layer insulating film formed on said first inter-layer insulating film, wherein said second inter-layer insulating film includes up to five layers;

a third connection hole which reaches said plug and is formed through said second inter-layer insulating film; and

a conductive portion which is connected to said plug and formed in said third connection hole, wherein said plug and said conductive portion are a storage node contact portion of a dynamic random access memory.

4. (CURRENTLY AMENDED) A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

a first inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said first inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said first inter-layer insulation film;

a plug having conductivity and filling internal portions of said first connection

hole and said second connection hole, wherein the upper surface of said plug is formed to almost the same height as the surface height of said first inter-layer insulating film;

a second inter-layer insulating film formed on said first inter-layer insulating film, wherein said second inter-layer insulating film includes up to five layers;

a third connection hole which reaches said plug and is formed through said second inter-layer insulating film; and

a conductive contact portion which is connected to said plug and formed in said third connection hole, wherein said plug and said conductive portion are a storage node contact portion of a dynamic random access memory.

5. (CANCELED).

6. (CANCELED).